REMARKS

This is in response to the Office Action dated November 8, 2006. Claims 1-3 and 5-23 are pending.

Section 112 Rejection

Claim 1 stands rejected under Section 112, first paragraph. In particular, the Office Action contends that "connected directly in series" as recited in claim 1 is not supported by the specification as originally filed. This Section 112 rejection is respectfully traversed.

Claim 1 requires that (a) *the first and second PMOS transistors are connected directly in series,* and/or (b) *the first and second NMOS transistors are connected directly in series.* These recitations are supported by the instant specification as originally filed, at least via the figures thereof. For example and without limitation, figures of the instant application illustrate a cell which includes PMOS section M05 comprising *PMOS transistors M05a and M05b connected directly in series*, and an NMOS section M06 including *NMOS transistors M06a and M06b connected directly in series* (e.g., see Figs. 2B, 5B, 10B, 13B-15B, etc.). The figures, which are part of the specification, clearly show and thus describe these features. There is no requirement that a feature shown in the drawings also be described in text – this would be virtually impossible in many instances. Thus, it is respectfully submitted that the instant specification supports the claim language which requires that (a) the first and second PMOS transistors are connected directly in series, and/or (2) the first and second NMOS transistors are connected directly in series.

The Section 112 rejection is improper and should be withdrawn.

Art Rejection

Claim 1 stands rejected under Section 102(e) as being allegedly anticipated by Yoon. This Section 102(e) rejection is respectfully traversed for at least the following reasons.

Claim 1 requires that (a) *the first and second PMOS transistors are connected directly in series,* and/or (b) *the first and second NMOS transistors are connected directly in series.* This language in claim 1 prevents the Examiner from contending that in Fig. 6 of Yoon elements M16 and M19N are the claimed first and second NMOS transistors, and/or from contending that M15 and M19P are the claimed first and second PMOS transistors.

To summarize, Yoon fails to disclose or suggest that (1) *the first and second NMOS transistors are directly connected to each other in series* and/or (2) *the first and second PMOS transistors are directly connected to each other in series*, as required by claim 1. Instead, in Fig. 6 of Yoon, the PMOS transistor M15 of M16 and the PMOS transistor M19P are *not* connected directly in series; they are not connected directly in series because inverter devices M17, M18 and driver-register circuit 618 are provided therebetween. Moreover, in Fig. 6 of Yoon, NMOS transistors M16 and M19N are not connected directly in series because driver-register circuit 618 is provided therebetween. Moreover, one of ordinary skill in the art would never have removed elements 618, M18 and M18 from Fig. 6 of Yoon.

Conclusion

It is respectfully requested that all rejections be withdrawn. Claims 1, 6 and 8 are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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By: _____

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